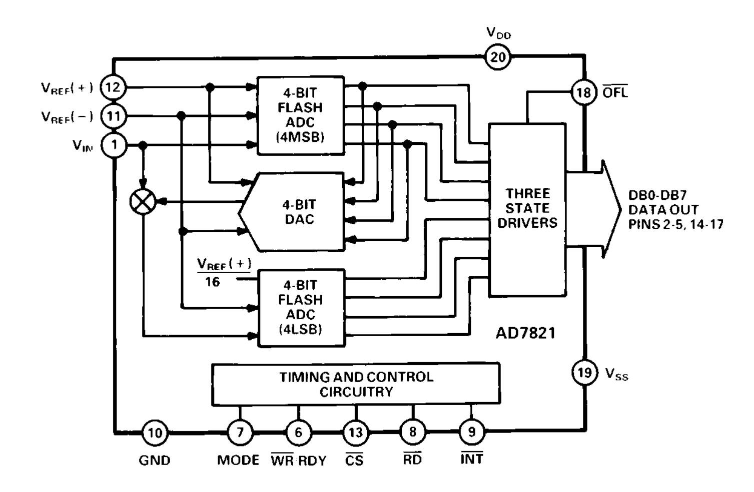


LC²MOS High Speed, μP-Compatible 8-Bit ADC with Track/Hold Function

AD7821

FEATURES
Fast Conversion Time: 660 ns max
100 kHz Track-and-Hold Function
1 MHz Sample Rate
Unipolar and Bipolar Input Ranges
Ratiometric Reference Inputs
No External Clock
Extended Temperature Range Operation
Skinny 20-Pin DIPs, SOIC and 20-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7821 is a high speed, 8-bit, sampling, analog-to-digital converter that offers improved performance over the popular AD7820. It offers a conversion time of 660 ns (vs. 1.36 μs for the AD7820) and 100 kHz signal bandwidth (vs. 6.4 kHz). The sampling instant is better defined and occurs on the falling edge of $\overline{WR}$ or $\overline{RD}$. The provision of a V_{SS} pin (Pin 19) allows the part to operate from ±5 V supplies and to digitize bipolar input signals. Alternatively, for unipolar inputs, the V_{SS} pin can be grounded and the AD7821 will operate from a single +5 V supply, like the AD7820.

The AD7821 has a built-in track-and-hold function capable of digitizing full-scale signals up to 100 kHz max. It also uses a half-flash conversion technique that eliminates the need to generate a CLK signal for the ADC.

The AD7821 is designed with standard microprocessor control signals ($\overline{CS}$, $\overline{RD}$, $\overline{WR}$, RDY, $\overline{INT}$) and latched, three-state data outputs capable of interfacing to high speed data buses. An overflow output ($\overline{OFL}$) is also provided for cascading devices to achieve higher resolution.

The AD7821 is fabricated in Linear-Compatible CMOS (LC²MOS), an advanced, mixed technology process combining precision bipolar circuits with low power CMOS logic. The part features a low power dissipation of 50 mW.

PRODUCT HIGHLIGHTS

1. Fast Conversion Time
   The half-flash conversion technique, coupled with fabrication on Analog Devices' LC²MOS process, enables a very fast conversion time. The conversion time for the WR-RD mode is 660 ns, with 700 ns for the RD mode.
2. Built-In Track-and-Hold
   This allows input signals with slew rates up to 1.6 V/μs to be converted to 8-bits without an external track-and-hold. This corresponds to a 5 V peak-to-peak, 100 kHz sine wave signal.
3. Total Unadjusted Error
   The AD7821 features an excellent total unadjusted error figure of less than ±1 LSB over the full operating temperature range.
4. Unipolar/Bipolar Input Ranges
   The AD7821 is specified for single supply (+5 V) operation with a unipolar full-scale range of 0 to +5 V, and for dual supply (±5 V) operation with a bipolar input range of ±2.5 V. Typical performance characteristics are given for other input ranges.
5. Dynamic Specifications for DSP Users
   In addition to the traditional ADC specifications, the AD7821 is specified for ac parameters, including signal-to-noise ratio, distortion and slew rate.

REV. A

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AD7821–SPECIFICATIONS

V_{DD} = +5 V ± 5%, GND = 0 V. Unipolar Input Range: V_{SS} = GND, $V_{REF}(+)$ = 5 V, $V_{REF}(–)$ = GND. Bipolar Input Range: V_{SS} = –5 V ± 5%, $V_{REF}(+)$ = 2.5 V, $V_{REF}(–)$ = –2.5 V. These test conditions apply unless otherwise stated. All specifications T_{MIN} to T_{MAX} unless otherwise noted. Specifications apply for RD Mode (Pin 7 = 0 V).

Parameter	K Version[1]	B, T Versions	Units	Comments
UNIPOLAR INPUT RANGE				
Resolution[2]	8	8	Bits	
Total Unadjusted Error[3]	±1	±1	LSB max	
Minimum Resolution for which No Missing Codes are Guaranteed	8	8	Bits	
BIPOLAR INPUT RANGE				
Resolution[2]	8	8	Bits	
Zero Code Error	±1	±1	LSB max	
Full Scale Error	±1	±1	LSB max	
Signal-to-Noise Ratio (SNR)[3]	45	45	dB min	V_{IN} = 99.85 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 500 kHz
Total Harmonic Distortion (THD)[3]	–50	–50	dB max	V_{IN} = 99.85 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 500 kHz
Peak Harmonic or Spurious Noise[3]	–50	–50	dB max	V_{IN} = 99.85 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 500 kHz
Intermodulation Distortion (IMD)[3]				fa (84.72 kHz) and fb (94.97 kHz) Full-Scale Sine Waves with $f_{SAMPLING}$ = 500 kHz
	–50	–50	dB max	Second Order Terms
	–50	–50	dB max	Third Order Terms
Slew Rate, Tracking[3]	1.6	1.6	V/µs max	
	2.36	2.36	V/µs typ	
REFERENCE INPUT				
Input Resistance	1.0/4.0	1.0/4.0	kΩ min/kΩ max	
$V_{REF}(+)$ Input Voltage Range	$V_{REF}(–)/V_{DD}$	$V_{REF}(–)/V_{DD}$	V min/V max	
$V_{REF}(–)$ Input Voltage Range	$V_{SS}/V_{REF}(+)$	$V_{SS}/V_{REF}(+)$	V min/V max	
ANALOG INPUT				
Input Voltage Range	$V_{REF}(–)/V_{REF}(+)$	$V_{REF}(–)/V_{REF}(+)$	V min/ max	
Input Leakage Current	±3	±3	µA max	–5 V ≤ V_{IN} ≤ +5 V
Input Capacitance	55	55	pF typ	
LOGIC INPUTS				
$\overline{CS}$, $\overline{WR}$, $\overline{RD}$				
V_{INH}	2.4	2.4	V min	
V_{INL}	0.8	0.8	V max	
I_{INH} ($\overline{CS}$, $\overline{RD}$)	1	1	µA max	
I_{INH} ($\overline{WR}$)	3	3	µA max	
I_{INL}	–1	–1	µA max	
Input Capacitance[4]	8	8	pF max	Typically 5 pF
MODE				
V_{INH}	3.5	3.5	V min	
V_{INL}	1.5	1.5	V max	
I_{INH}	200	200	µA max	50 µA typ
I_{INL}	–1	–1	µA max	
Input Capacitance[4]	8	8	pF max	Typically 5 pF
LOGIC OUTPUTS				
DB0–DB7, $\overline{OFL}$, $\overline{INT}$				
V_{OH}	4.0	4.0	V min	I_{SOURCE} = 360 µA
V_{OL}	0.4	0.4	V max	I_{SINK} = 1.6 mA
I_{OUT} (DB0–DB7)	±3	±3	µA max	Floating State Leakage
Output Capacitance[4] (DB0–DB7)	8	8	pF max	Typically 5 pF
RDY				
V_{OL}	0.4	0.4	V max	I_{SINK} = 2.6 mA
I_{OUT}	±3	±3	µA max	Floating State Leakage
Output Capacitance[4]	8	8	pF max	Typically 5 pF
POWER SUPPLY				
I_{DD}[5]	15	20	mA max	$\overline{CS}$ = $\overline{RD}$ = 0 V
I_{SS}	100	100	µA max	$\overline{CS}$ = $\overline{RD}$ = 0 V
Power Dissipation	50	50	mW typ	
Power Supply Sensitivity	±1/4	±1/4	LSB max	±1/16 LSB typ, V_{DD} = 4.75 V to 5.25 V, ($V_{REF}(+)$ = 4.75 V max for Unipolar Mode)

NOTES

[1]Temperature Ranges are as follows: K Version = –40°C to +85°C; B Version = –40°C to +85°C; T Version = –55°C to +125°C.

[2]1 LSB = 19.53 mV for both the unipolar (0 V to +5 V) and bipolar (–2.5 V to +2.5 V) input ranges.

[3]See Terminology.

[4]Sample tested at +25°C to ensure compliance.

[5]See Typical Performance Characteristics.

Specifications subject to change without notice.

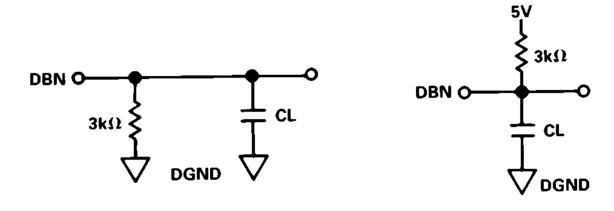
TIMING CHARACTERISTICS[1] (V_{DD} = +5 V ± 5%, V_{SS} = 0 V or –5 V ± 5%; Unipolar or Bipolar Input Range)

Parameter	Limit at +25°C (All Versions)	Limit at T_{MIN}, T_{MAX} (K, B Versions)	Limit at T_{MIN}, T_{MAX} (T Version)	Units	Conditions/Comments
t_{CSS}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}/\overline{WR}$ Setup Time
t_{CSH}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}/\overline{WR}$ Hold Time
t_{RDY}[2]	70	85	100	ns max	$\overline{CS}$ to RDY Delay. Pull-Up Resistor 5 k1.
t_{CRD}	700	875	975	ns max	Conversion Time (RD Mode)
t_{ACC0}[3]					Data Access Time (RD Mode)
	t_{CRD} + 25	t_{CRD} + 30	t_{CRD} + 35	ns max	C_L = 20 pF
	t_{CRD} + 50	t_{CRD} + 65	t_{CRD} + 75	ns max	C_L = 100 pF
t_{INTH}[2]	50	–	–	ns typ	$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)
	80	85	90	ns max	
t_{DH}[4]	15	15	15	ns min	Data Hold Time
	60	70	80	ns max	
t_P	350	425	500	ns min	Delay Time Between Conversions
t_{WR}	250	325	400	ns min	Write Pulse Width
	10	10	10	µs max	
t_{RD}	250	350	450	ns min	Delay Time between $\overline{WR}$ and $\overline{RD}$ Pulses
t_{READ1}	160	205	240	ns min	$\overline{RD}$ Pulse Width (WR-RD Mode, see Figure 12b) Determined by t_{ACC1}
t_{ACC1}[3]					Data Access Time (WR-RD Mode, see Figure 12b)
	160	205	240	ns max	C_L = 20 pF
	185	235	275	ns max	C_L = 100 pF
t_{RI}	150	185	220	ns max	$\overline{RD}$ to $\overline{INT}$ Delay
t_{INTL}[2]	380	–	–	ns typ	$\overline{WR}$ to $\overline{INT}$ Delay
	500	610	700	ns max	
t_{READ2}	65	75	85	ns min	$\overline{RD}$ Pulse Width (WR-RD Mode, see Figure 12a) Determined by t_{ACC2}
					Data Access Time (WR-RD Mode, see Figure 12a)
t_{ACC2}[3]	65	75	85	ns max	C_L = 20 pF
	90	110	130	ns max	C_L = 100 pF
t_{IHWR}[2]	80	100	120	ns max	$\overline{WR}$ to $\overline{INT}$ Delay (Stand-Alone Operation)
t_{ID}[3]					Data Access Time after $\overline{INT}$ (Stand-Alone Operation)
	30	35	40	ns max	C_L = 20 pF
	45	60	70	ns max	C_L = 100 pF

NOTES
[1]Sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.
[2]C_L = 50 pF.
[3]Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[4]Defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.

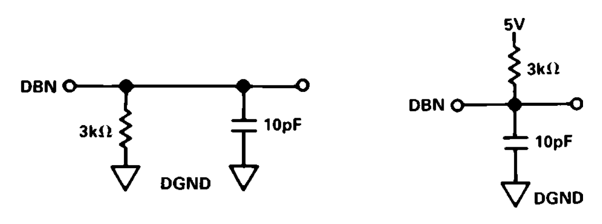
Specifications subject to change without notice.

Test Circuits



a. High Z to V_{OH} *b. High Z to V_{OL}*

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High Z *b. V_{OL} to High Z*

Figure 2. Load Circuits for Data Hold Time Test

ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error (LSB)	Package Option[2]
AD7821KN	–40°C to +85°C	±1 max	N-20
AD7821KP	–40°C to +85°C	±1 max	P-20A
AD7821KR	–40°C to +85°C	±1 max	R-20
AD7821BQ	–40°C to +85°C	±1 max	Q-20
AD7821TQ	–55°C to +125°C	±1 max	Q-20
AD7821TE	–55°C to +125°C	±1 max	E-20A

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact local sales office for military data sheet.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND . . . . –0.3 V, + 7 V
V_{SS} to GND . . . . +0.3 V, + 7 V
Digital Input Voltage to GND
  (Pins 6–8, 13) . . . . –0.3 V, V_{DD} + 0.3 V
Digital Output Voltage to GND
  (Pins 2–5, 9, 14–18) . . . . –0.3 V, V_{DD} + 0.3 V
$V_{REF}(+)$ to GND . . . . V_{SS} – 0.3 V, V_{DD} + 0.3 V
$V_{REF}(–)$ to GND . . . . V_{SS} – 0.3 V, V_{DD} + 0.3 V
V_{IN} to GND . . . . V_{SS} – 0.3 V, V_{DD} + 0.3 V
Operating Temperature Range
  Commercial (K Version) . . . . –40°C to +85°C
  Industrial (B Version) . . . . –40°C to +85°C
  Extended (T Version) . . . . –55°C to +125°C
Storage Temperature Range . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . 450 mW
Derates above +75°C by . . . . 6 mW/°C

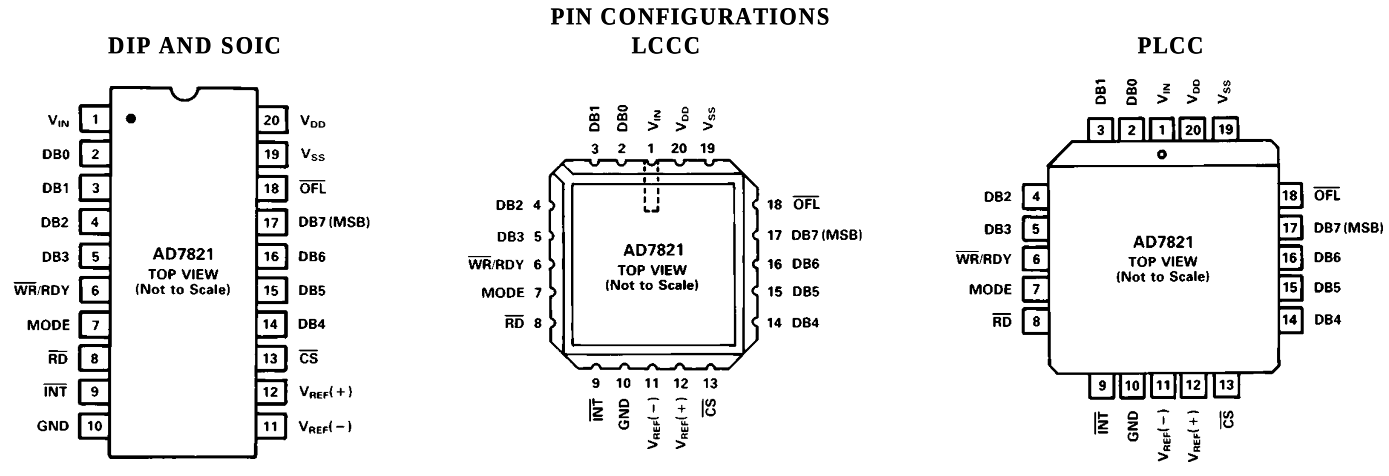
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7821 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATIONS



TERMINOLOGY

LEAST SIGNIFICANT BIT (LSB)

An ADC with 8-bit resolution can resolve one part in 2^8 (1/256 of full scale). For the AD7821 operating in either the unipolar or bipolar input range with 5 V full scale, one LSB is 19.53 mV.

TOTAL UNADJUSTED ERROR

This is a comprehensive specification which includes relative accuracy, offset error and full-scale error.

SLEW RATE

Slew Rate is the maximum allowable rate of change of input signal such that the digital sample values are not in error.

TOTAL HARMONIC DISTORTION

Total harmonic distortion is the ratio of the square root of the sum of the squares of the rms value of the harmonics to the rms value of the fundamental. For the AD7821, total harmonic distortion (THD) is defined as

$$20\ log\left[\frac{\sqrt{\left(V_2^{\,2}+V_3^{\,2}+V_5^{\,2}+V_6^{\,2}\right)}}{V_1}\right]dB$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, V_6, are the rms amplitudes of the individual harmonics.

INTERMODULATION DISTORTION

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mfa+nfb, where m, n = 0, 1, 2, 3,- - - -. Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), and the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb). For the AD7821 intermodulation distortion is calculated separately for both the second and third order terms.

SIGNAL-TO-NOISE RATIO

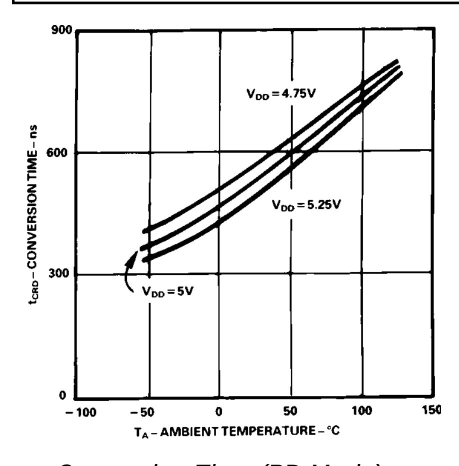
Signal-to-noise ratio (SNR) is measured signal-to-noise at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all nonfundamental signals (excluding dc) up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process. The theoretical SNR for a sine wave input is given by:

$$SNR = (6.02\ N + 1.76)\ dB$$

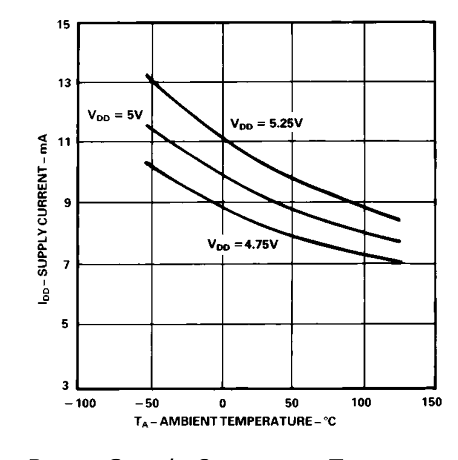
where N is the number of bits in the ADC. Thus, for an ideal 8-bit ADC, SNR = 50 dB.

PEAK HARMONIC OR SPURIOUS NOISE

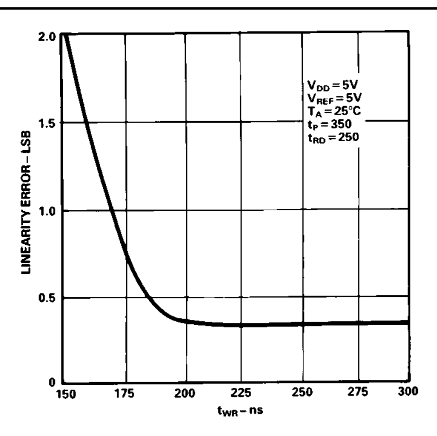
Peak harmonic or spurious noise is the rms value of the largest nonfundamental frequency (excluding dc) up to half the sampling frequency to the rms value of the fundamental.



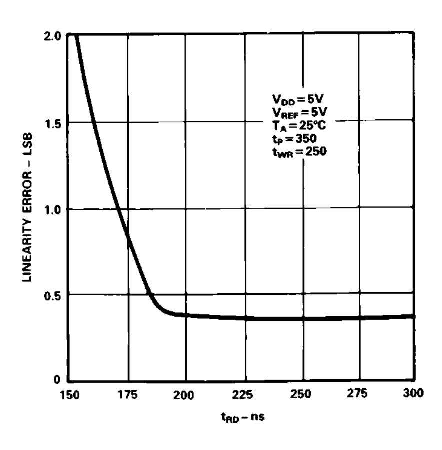
Conversion Time (RD Mode) vs. Temperature



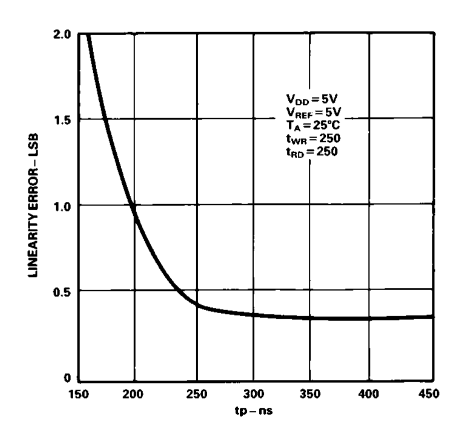
Power Supply Current vs. Temperature (Not Including Reference Ladder)



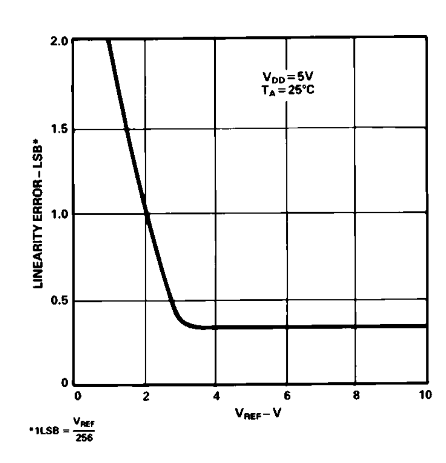
Accuracy vs. t_{WR}



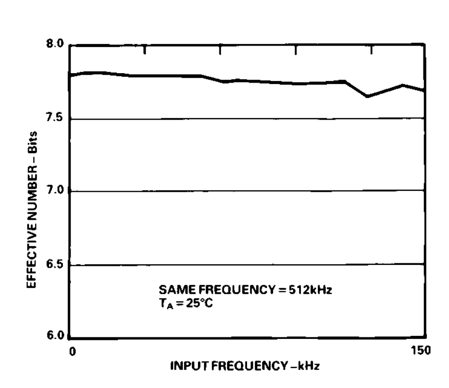
Accuracy vs. t_{RD}



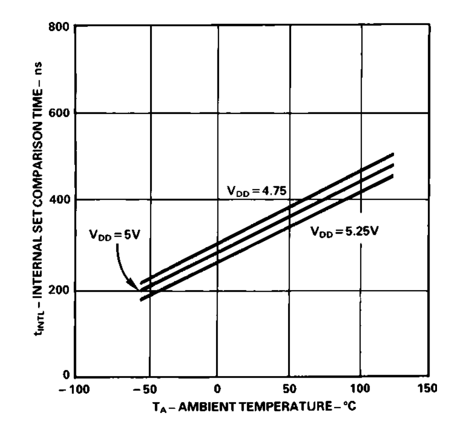
Accuracy vs. t_P



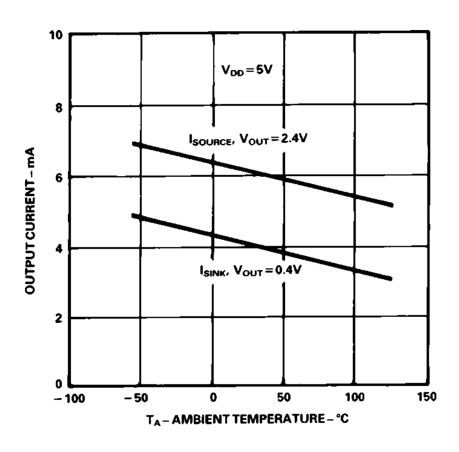
Accuracy vs. V_{REF} [$V_{REF} = V_{REF}(+) – V_{REF}(–)$]



Effective Number of Bits vs. Input Signal (±2.5 V) Frequency



t_{INTL}, Internal Time Delay vs. Temperature



Output Current vs. Temperature

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	V_{IN}	Analog Input: Range $V_{REF}(-) \le V_{IN} \le V_{REF}(+)$
2	DB0	Three-State Data Output (LSB).
3–5	DB1–DB3	Three-State Data Outputs.
6	$\overline{WR}$/RDY	WRITE control input/READY status output. See Digital Interface section.
7	MODE	Mode Selection Input. It determines whether the device operates in the WR-RD or RD mode. This input is internally pulled low through a 50 μA current source. See Digital Interface section.
8	$\overline{RD}$	READ Input. $\overline{RD}$ must be low to access data from the part. See Digital Interface section.
9	$\overline{INT}$	INTERRUPT Output. $\overline{INT}$ going low indicates that the conversion is complete. $\overline{INT}$ returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$. See Digital Interface section.
10	GND	Ground.
11	$V_{REF}(-)$	Lower limit of reference span. Range: $V_{SS} \le V_{REF}(-) \le V_{REF}(+)$.
12	$V_{REF}(+)$	Upper limit of reference span. Range: $V_{REF}(-) < V_{REF}(+) \le V_{DD}$.
13	$\overline{CS}$	Chip Select Input. The device is selected when this input is low.
14–16	DB4–DB6	Three-State Data Outputs.
17	DB7	Three-State Data Output (MSB).
18	$\overline{OFL}$	Overflow Output. If the analog input is higher than ($V_{REF}(+)$ – 1/2 LSB), $\overline{OFL}$ will be low at the end of conversion. It is a non-three-state output which can be used to cascade 2 or more devices to increase resolution.
19	V_{SS}	Negative supply voltage. V_{SS} = 0 V; Unipolar Operation. V_{SS} = –5 V; Bipolar Operation.
20	V_{DD}	Positive supply voltage, +5 V.

CIRCUIT INFORMATION

BASIC DESCRIPTION

The AD7821 uses a half flash conversion technique (see Functional Block Diagram), whereby two 4-bit flash ADCs are used to achieve an 8-bit result. Each 4-bit flash ADC contains 15 comparators, which compare an unknown input voltage to the reference ladder, to achieve a 4-bit result. The MS (most significant) flash ADC converts an unknown analog input voltage (V_{IN}) to provide the 4 MS data bits. An internal DAC, driven by the 4 MS data bits, then recreates an analog approximation of the input voltage. The DAC output voltage is subtracted from the analog input, and the difference is converted by the LS (least significant) ADC to provide the 4 LS data bits. The MS flash ADC also has one additional comparator to detect overrange on the analog input.

OPERATING SEQUENCE

The AD7821 has two operating modes. The RD mode allows a conversion to be started and data to be read with a single, extended, READ operation (i.e., $\overline{CS}$ and $\overline{RD}$ are taken low). The conversion process is timed out by internal one-shots. The WR-RD mode uses $\overline{WR}$ to start a conversion and $\overline{RD}$ to read the data and allows the conversion timing to be externally controlled. The operating sequence for the WR-RD mode is shown in Figure 3.

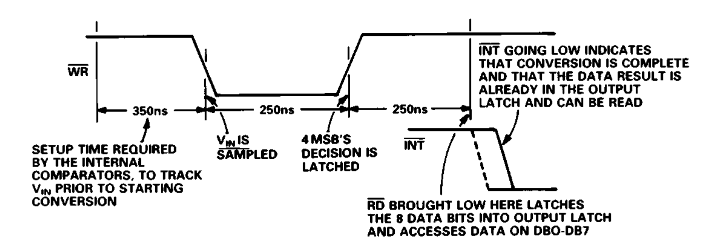


Figure 3. Operating Sequence (WR-RD Mode)

A conversion is initiated and the analog input signal (V_{IN}) sampled on the falling edge of $\overline{WR}$ (falling edge of $\overline{RD}$, RD mode). A setup time (t_P, delay time between conversions) of 350 ns is required prior to this falling edge. See Digital Interface section for more details. When $\overline{WR}$ is low, the internal MS (most significant) ADC compares the sampled analog input with the reference ladder to provide the 4 MS data bits. A minimum of 250 ns is required for this comparison. On the rising edge of $\overline{WR}$, the MS data result is latched internally and the LS (least significant) conversion begins, to yield the 4 LS data bits. $\overline{INT}$ goes low typically 380 ns after the rising edge of $\overline{WR}$. This indicates the LS conversion is complete and that both the LS and MS data results are latched into the output buffer. $\overline{RD}$ going low then enables the output data. If a faster conversion time is required, the $\overline{RD}$ line can be brought low 250 ns after $\overline{WR}$ goes high. This latches both the LS and MS data bits and outputs the conversion result on DB0–DB7.

REFERENCE AND INPUT

The $V_{REF}(-)$ and $V_{REF}(+)$ reference inputs on the AD7821 are fully differential and define the zero and full-scale input range of the ADC. The transfer characteristic of the part is defined by the integer value of the following expression:

$$Data\ \ (LSBs) = 256\left[\frac{V_{IN} - V_{REF}(-)}{V_{REF}(+) - V_{REF}(-)}\right] + 0.5$$

As a result, the analog input (V_{IN}) Of the device can easily be set up to provide both unipolar and bipolar operation. The data output code for unipolar and bipolar operation is Natural Binary and Offset Binary, respectively.

The span of the analog input voltage can easily be varied. By reducing the reference span, $V_{REF}(+) - V_{REF}(-)$, to less than 5 V the sensitivity of the converter can be increased (i.e., if V_{REF} = 2 V then 1 LSB = 7.8 mV). The reference flexibility also allows the input span for unipolar operation to be offset from zero ($V_{REF}(-)$ > GND). Additionally, the input/reference arrangement facilitates ratiometric operation.

Figures 4 and 5 show some configurations which are possible. For minimum noise a 47 μF capacitor in parallel with a 0.1 μF capacitor should be connected between the reference inputs and GND.

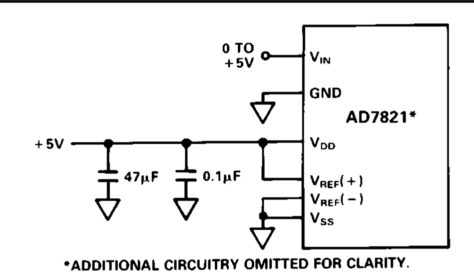


Figure 4. Power Supply as Reference. Unipolar Operation (0 to + 5 V)

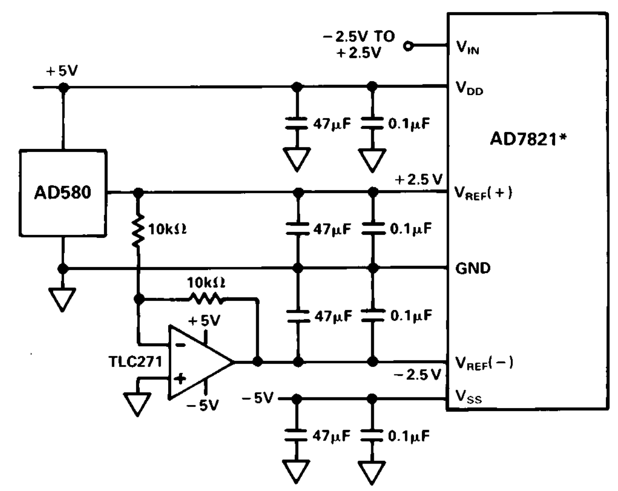


Figure 5. External Reference. Bipolar Operation (–2.5 V to +2.5 V)

INPUT CURRENT

The analog input of the AD7821 behaves somewhat differently to conventional A/D converters. This is due to the ADC's sampled data comparators, which take varying amounts of input current depending on the cycle of the converter.

The equivalent input circuit of the AD7821 is shown in Figure 6. When a conversion ends (e.g., falling edge of $\overline{INT}$, WR-RD mode, $t_{RD} > t_{INTL}$) all the input switches are closed and V_{IN} is connected to the comparators of the internal LS and MS ADCs. Therefore, V_{IN} is connected to 31 one-pF input capacitors simultaneously .

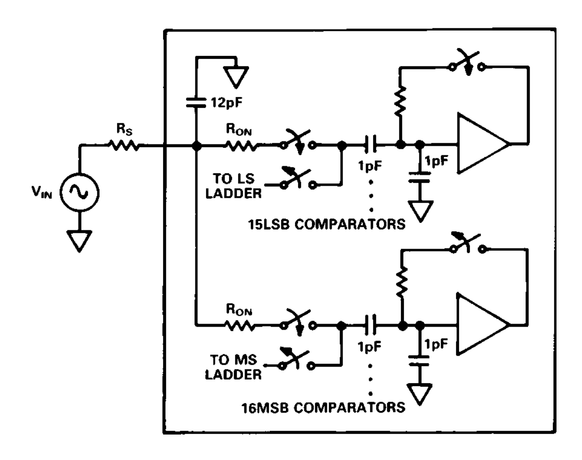


Figure 6. AD7821 Equivalent Input Circuit

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 2 kΩ to 5 kΩ). In addition, about 12 pF of input stray capacitance must be charged.

The analog input can be modeled as an equivalent RC network as shown in Figure 7. As R_S (source impedance) increases, the input capacitance takes longer to charge.

The comparators track the analog input between conversions. A minimum delay time (t_P) of 350 ns is required between conversions to allow for voltage source settling and comparator tracking time. This allows input time constants of 50 ns without settling time problems. Typical total input capacitance values of 55 pF allow R_S to be 0.9 kΩ without lengthening t_P to give V_{IN} more time to settle.

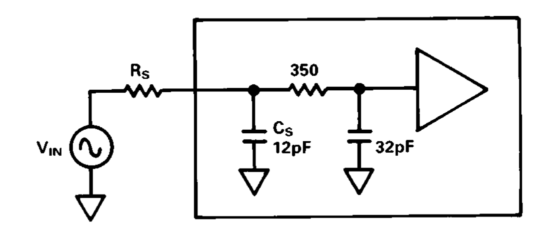


Figure 7. RC Network Model

INPUT TRANSIENTS

Transients on the analog input signal caused by charging current flowing into V_{IN} will not normally degrade the ADC's performance. In effect, the AD7821 does not "look" at the input when these transients occur. The comparators' inputs track V_{IN} and are not sampled until the falling edge of $\overline{WR}$ (WR-RD Mode) or $\overline{RD}$ (RD Mode), so at least 350 ns (t_P) is provided to charge the ADC's input capacitance. It is, therefore, not necessary to filter out these transients with an external capacitor at the V_{IN} terminal.

INHERENT TRACK-AND-HOLD

A major benefit of the AD7821's input structure is its ability to measure a variety of high-speed signals without the help of an external track-and-hold. Any ADC which does not have a built-in track-and-hold, regardless of its speed, requires the analog input to remain stable to at least 1/2 LSB for the duration of the conversion to maintain full accuracy. This requires the use of a track-and-hold whenever the input is a high-speed signal. The AD7821's sampled-data comparators, by nature of their input switching, inherently accomplish this track-and-hold function. Although the conversion time for the AD7821 is 660 ns (WR-RD mode, $t_{WR} + t_{RD} + t_{ACC1}$), the time for which V_{IN} must be stable to 1/2 LSB is much smaller. The AD7821 tracks V_{IN} between conversions only, and its value on the falling edge of $\overline{WR}$ or $\overline{RD}$ in the WR-RD or RD modes, respectively, is the measured value.

SINUSOIDAL INPUTS

The bandwidth of the built-in track-and-hold is 100 kHz max (150 kHz typ, 5 V p-p). This is limited by the analog bandwidth of the comparators and timing skew between the comparator switches. This means that the analog input frequency can be up to 100 kHz without the aid of an external track-and-hold. The Nyquist criterion requires that the sampling rate be at least twice the input frequency (i.e., ≥2 × 100 kHz). This requires an ideal antialiasing filter with an infinite roll-off. To ease the prob-

lem of antialiasing filter design, the sampling rate is usually set much greater than the Nyquist criterion. The maximum sampling rate (f_{MAX}) for the AD7821 in the WR-RD mode, ($t_{RD} < t_{INTL}$) can be calculated as follows:

$$f_{MAX} = \frac{1}{t_{WR} + t_{RD} + t_{RI} + t_P}$$

$$f_{MAX} = \frac{1}{0.25E-6 + 0.25E-6 + 0.15E-6 + 0.35E-6}$$

t_{WR} = *Write Pulse Width*

t_{RD} = *Delay Time between* $\overline{WR}$ *and* $\overline{RD}$ *Pulses*

t_{RI} = $\overline{RD}$ *to* $\overline{INT}$ *Delay*

t_P = *Delay Time between Conversions*

This permits a maximum sampling rate for the AD7821 of 1 MHz, which is much greater than the Nyquist criterion for sampling a 100 kHz analog input signal.

DIGITAL SIGNAL PROCESSING APPLICATIONS

In Digital Signal Processing (DSP) application areas like voice recognition, echo cancellation and adaptive filtering, the dynamic characteristics (Signal-to-Noise Ratio, Harmonic Distortion, Intermodulation Distortion) of an ADC are critical. Since the AD7821 is a very fast ADC with a built-in track-and-hold function, it is specified dynamically as well as with standard dc specifications (Total Unadjusted Error, etc.).

SIGNAL-TO-NOISE RATIO AND DISTORTION

The dynamic performance of the AD7821 is evaluated by applying a very low distortion sine wave signal to the analog input (V_{IN}) which is then sampled at a 512 kHz sampling rate. A Fast Fourier Transform (FFT) plot is then generated from which Signal-to-Noise Ratio (SNR) and harmonic distortion data are obtained.

Figure 8 shows a 2048 point FFT plot of the AD7821 with an input signal of 100.25 kHz. The SNR is 49.1 dB. It should be noted that the harmonics are taken into account when calculating the SNR. The theoretical relationship between SNR and resolution (N) is expressed by the following equation:

$$SNR = (6.02\,N + 1.76)\,dB \qquad (1)$$

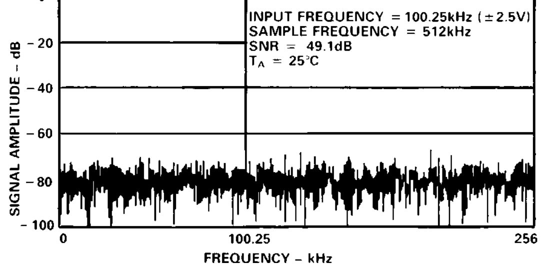


Figure 8. AD7821 FFT Plot

EFFECTIVE NUMBER OF BITS

By working backwards from Equation (1) it is possible to get a measure of ADC performance expressed in effective number of bits (N). A plot of the effective number of bits versus input frequency is given in the Typical Performance Characteristics section. The effective number of bits typically falls between 7.7 and 7.9, corresponding to SNR figures of 48.1 and 49.7 dB.

INTERMODULATION DISTORTION

For intermodulation distortion (IMD), an FFT plot consisting of very low distortion sine waves at two frequencies is generated by sampling an analog input applied to the ADC. Figure 9 shows a 2048 point plot for IMD.

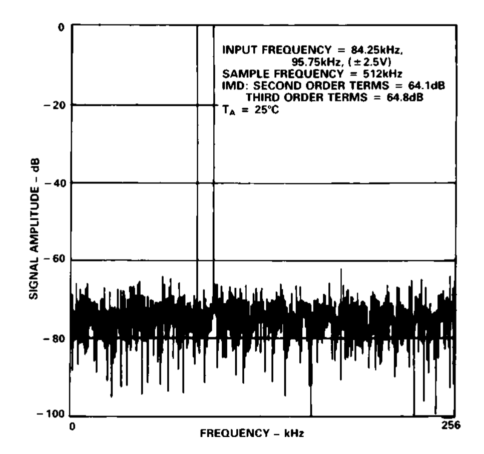


Figure 9. FFT Plot for IMD

HISTOGRAM PLOT

When a sine wave of specified frequency is applied to the V_{IN} input of the AD7821 and several thousand samples are taken, it is possible to plot a histogram showing the frequency of occurrence of each of the 256 ADC codes. A perfect ADC produces a probability density function described by the equation:

$$P(V) = \frac{1}{\pi(A^2 - V^2)^{1/2}}$$

where *A* is the peak amplitude of the sine wave and *P*(*V*) is the probability of occurrence at a voltage V.

If a particular step is wider than the ideal 1 LSB width, then the code associated with that step will accumulate more counts than for the code for an ideal step. Likewise, a step narrower than the ideal width will have fewer counts. Missing codes are easily seen because a missing code means zero counts for a particular code. The absence of large spikes in the plot indicates small differential nonlinearity.

Figure 10 shows a histogram plot for the AD7821, which corresponds very well with the ideal shape. The plot indicates very small differential nonlinearity and no missing codes for an input frequency of 100.25 kHz.

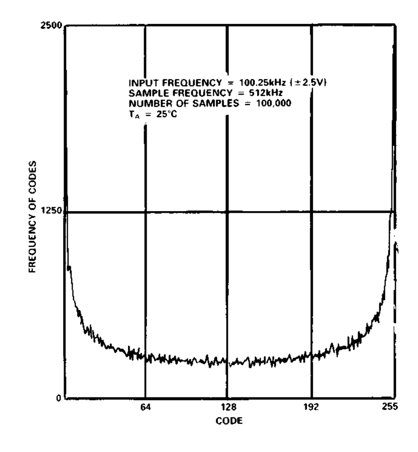


Figure 10. AD7821 Histogram Plot

In digital signal processing applications, where the AD7821 is used to sample ac signals, it is essential that the signal sampling occurs at exactly equal intervals. This minimizes errors due to sampling uncertainty or jitter. A precise timer or clock source, to start the ADC conversion process, is the best method of generating equidistant sampling intervals.

The two modes of operation given in the data sheet are suitable for DSP applications because the sampling instant of the AD7821 is well defined. V_{IN} is sampled on the falling edge of WR or RD in the WR-RD or RD modes, respectively.

DIGITAL INTERFACE

The AD7821 has two basic interface modes which are determined by the status of the MODE pin. When this pin is low, the converter is in the RD mode, with this pin high, the AD7821 is set up for the WR-RD mode.

The RD mode is designed for microprocessors that can be driven into a WAIT state. A READ operation (i.e., CS and RD are taken low) starts a conversion and data is read when the conversion is complete. The WR-RD mode does not require microprocessor WAIT states. A WRITE operation (i.e., CS and WR are taken low) initiates a conversion, and a READ operation reads the result when the conversion is complete.

RD Mode (MODE = 0)

The timing diagram for the RD mode is shown in Figure 11. This mode is intended for use with microprocessors which have a WAIT state facility, whereby a READ instruction cycle can be extended to accommodate slow memory devices. A conversion is started by taking CS and RD low (READ operation). Both CS and RD are then kept low until output data appears.

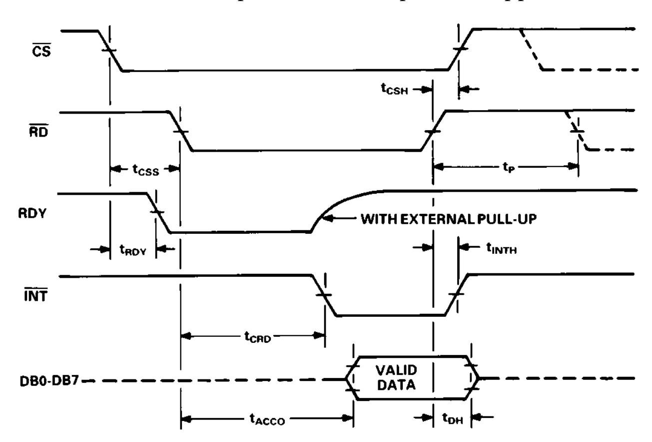


Figure 11. RD Mode

In this mode, Pin 6 of the AD7821 is configured as a status output, RDY. This RDY output can be used to drive the processor READY or WAIT input. It is an open drain output (no internal pull-up device) which goes low after the falling edge of CS and goes high impedance at the end of conversion. An INT line is also provided which goes low when a conversion is complete. INT returns high on the rising edge of CS or RD.

WR-RD Mode (MODE = 1)

In the WR-RD mode, Pin 6 is configured as a WRITE (WR) input for the AD7821. With CS low, conversion is initiated on the falling edge of WR. Two options exist for reading data from the converter.

In the first of these options the processor waits for the INT status line to go low before reading the data (see Figure 12a).

INT typically goes low within 380 ns after the rising edge of WR. It indicates that conversion is complete and that the data result is in the output latch. With CS low, the data outputs (DB0–DB7) are activated when RD goes low. INT is reset by the rising edge of RD or CS.

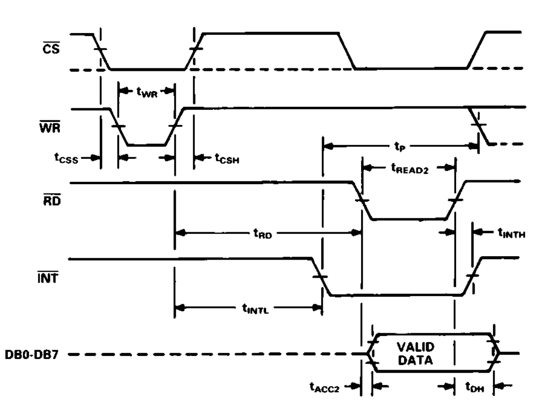


Figure 12a. WR-RD Mode ($t_{RD} > t_{INTL}$)

The alternative option can be used to shorten the conversion time. This is a method for bypassing the internal time-out circuit. The INT line is ignored and RD can be brought low 250 ns after the rising edge of WR. In this case RD going low transfers the data result into the output latch and activates the data output (DB0–DB7). INT is driven low on the falling edge of RD and is reset on the rising edge of RD or CS. The timing for this interface is shown in Figure 12b.

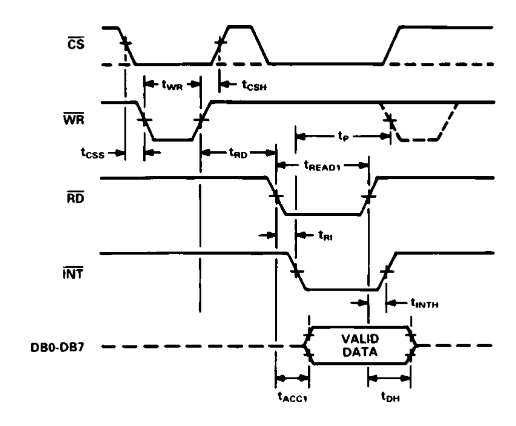


Figure 12b. WR-RD Mode ($t_{RD} < t_{INTL}$)

The AD7821 can also be used in stand-alone operation in the WR-RD mode. CS and RD are tied low, and a conversion is initiated by bringing WR low. Output data is valid 530 ns (t_{INTL} + t_{ID}) after the rising edge of WR. The timing diagram for this mode is shown in Figure 13.

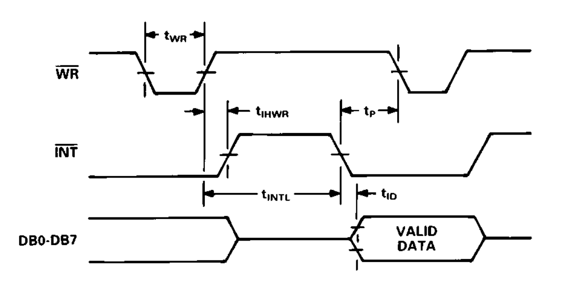


Figure 13. WR-RD Mode Stand-Alone Operation, CS = RD = 0

MICROPROCESSOR INTERFACING

The AD7821 is designed for easy interfacing to microprocessors as a memory mapped peripheral or an I/O device. This reduces to a minimum the amount of external logic required for interfacing.

AD7821 – 68008 INTERFACE

Figure 14 shows an AD7821 interface to the 68008 microprocessor. The ADC is configured for the RD interface mode. This means that one read instruction starts a conversion and reads the result when the conversion is completed. The read cycle is stretched out over the entire conversion period by taking the $\overline{INT}$ line back to the $\overline{DTACK}$ input of the 68008. Starting a conversion and reading the relevant data consists of a <MOVE B Dn, addr> instruction, where addr is the decoded ADC address and Dn is the data register into which the result is placed.

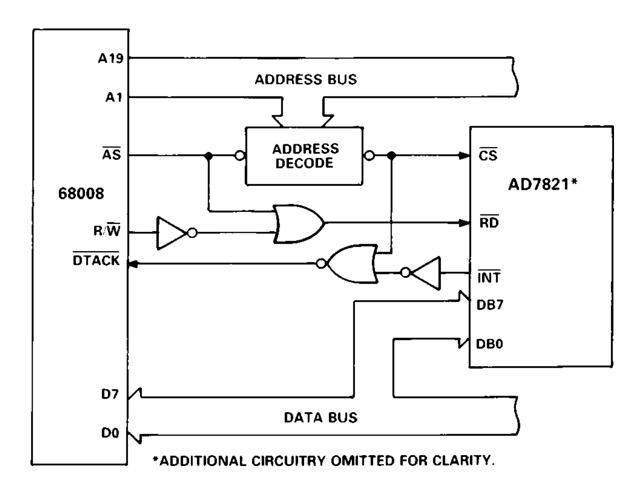


Figure 14. AD7821 to 68008 Interface

AD7821 – 8088 INTERFACE

A typical interface to the 8088 is shown in Figure 15. The AD7821 is configured for the RD interface mode. One read instruction starts a conversion and reads the result. The read cycle is stretched out over the entire conversion period by taking the RDY line back to the READY input of the 8088. Starting a conversion and reading the result consists of a <MOV AX, (addr)> instruction, where addr is the decoded ADC address and AX is the 8088 data register into which the conversion result is placed.

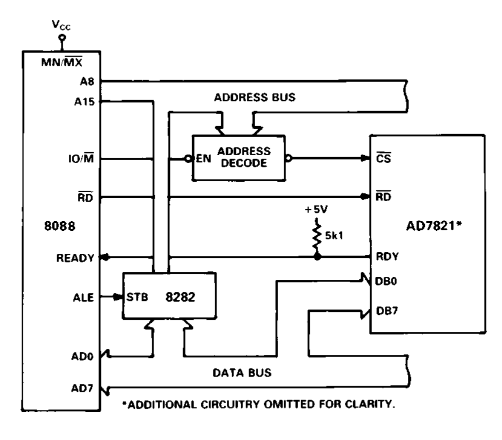


Figure 15. AD7821 to 8088 Interface

AD7821 – TMS32010 INTERFACE

A typical interface to the TMS32010 is shown in Figure 16. The AD7821 is mapped at a port address and the interface is designed for the maximum TMS32010 clock frequency of 20 MHz. In this case, the AD7821 is configured in the WR-RD interface mode. This means that a write instruction starts a conversion and a read instruction reads the result when the conversion is completed. A precise timer or clock source is used to start a conversion in applications requiring equidistant sampling intervals. The scheme used, whereby the AD7821 generates an interrupt to the TMS32010, is limited in that it does not allow the AD7821 to be sampled at its maximum rate. This is because the time between samples has to be long enough to allow the TMS32010 to service its interrupt and read data from the AD7821. Constant interruption of the TMS32010 by the AD7821, every time the ADC completes a conversion, is not a very efficient use of the processor time. To overcome these problems, some buffer memory or FIFO could be placed between the AD7821 and the TMS32010. The $\overline{INT}$ line of the AD7821 could be used to trigger a pulse which drives its $\overline{CS}$ and $\overline{RD}$ lines and places the AD7821 data into a FIFO or buffer memory. The microprocessor can then read a batch of data from the FIFO or buffer memory at some convenient time. Reading data from the AD7821, after an $\overline{INT}$ has been received, consists of <IN A, PA> instruction (PA is the decoded ADC address).

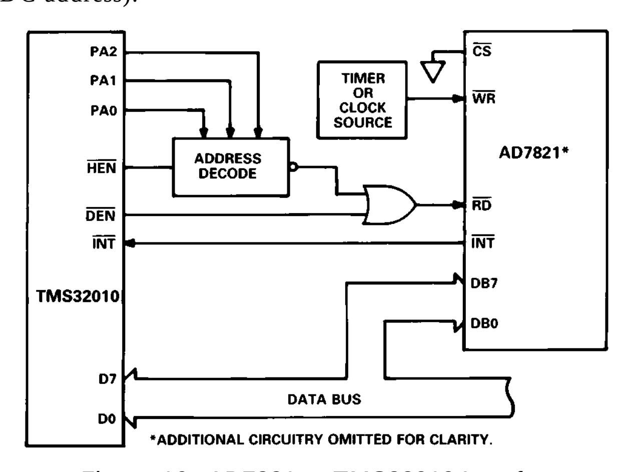


Figure 16. AD7821 to TMS32010 Interface

AD7821 – 8051 INTERFACE

Figure 17 shows the AD7821 interface to the 8051 microcomputer. The AD7821 is configured in the WR-RD interface mode and is connected to the 8051 ports. The processor starts conversion and then polls $\overline{INT}$, until it goes low, before reading the conversion result. Data is read from the AD7821 by using the <MOV A, 90H> instruction (90H is the address for Port 1).

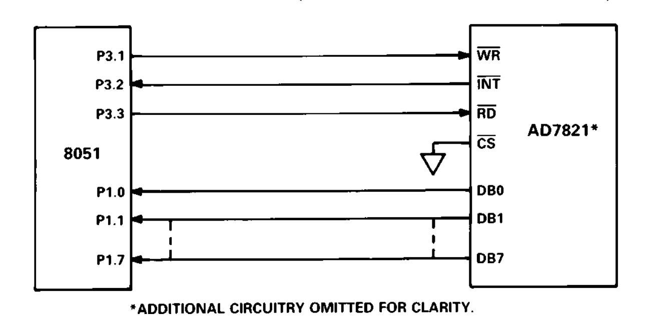


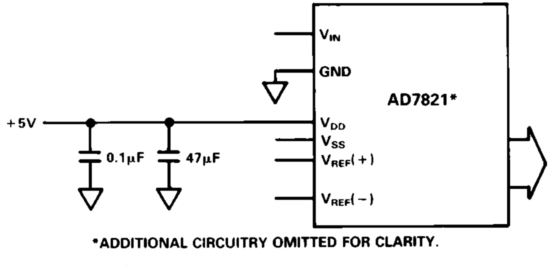
Figure 17. AD7821 to 8051 Interface

APPLYING THE AD7821

The AD7821 is specified for a unipolar input range of 0 to +5 V and a bipolar input range of –2.5 V to +2.5 V. The $V_{REF}(-)$ and $V_{REF}(+)$ voltages required for these input ranges are outlined below. See the Typical Performance Characteristics section for operation with unspecified input voltage ranges.

UNIPOLAR OPERATION

Figure 18 gives the configuration and reference voltages required for 0 V to +5 V operation. The nominal transfer characteristic for this input range is shown in Figure 19. The output code is Natural Binary with 1 LSB = (5/256) V = 19.5 mV.



*ADDITIONAL CIRCUITRY OMITTED FOR CLARITY.

$V_{REF}(+)$	$V_{REF}(-)$	V_{SS}	V_{IN}	RANGE
+5V	GND	GND	UNIPOLAR	0 to +5V
+2.5V	–2.5V	–5V	BIPOLAR	–2.5V to +2.5V

Figure 18. AD7821 Unipolar/Bipolar Operation

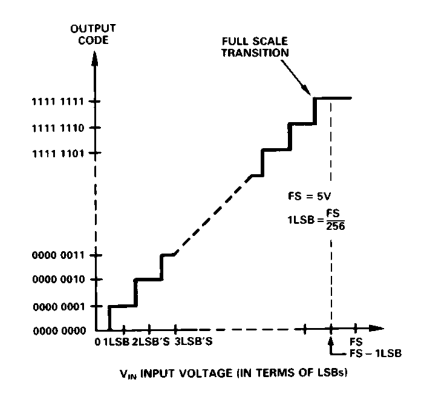


Figure 19. Nominal Transfer Characteristic for Unipolar (0 V to +5 V) Operation

BIPOLAR OPERATION

Figure 18 gives the configuration and reference voltages required for –2.5 V to +2.5 V operation. The nominal transfer characteristic for this input range is shown in Figure 20. The output code is Offset Binary with 1 LSB = ([+2.5 – (–2.5)]/256) V = 19.5 mV.

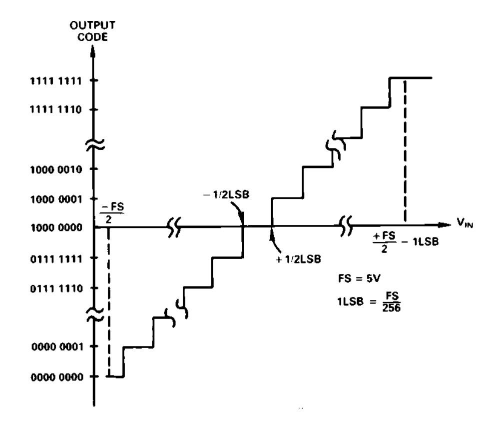


Figure 20. Nominal Transfer Characteristic for Bipolar (–2.5 V to +2.5 V) Operation

16-CHANNEL TELECOM A/D CONVERTER

The fast sampling rate (1 MHz) and bipolar operation of the AD7821 makes it useful in Telecom applications for sampling a number of input channels using a multiplexer. Figure 21 shows a circuit for such an application.

The maximum signal frequency required for acceptable quality in Telecom applications is 3 kHz. The circuit given in Figure 21 permits each of the 16-input channels to be sampled at a rate of 16 kHz maximum. The sampling rate takes account of such multiplexer parameters as t_{ON}, settling time etc. The circuit also eases the problem of the antialiasing filter design by sampling at a rate much greater than that required by the Nyquist criterion.

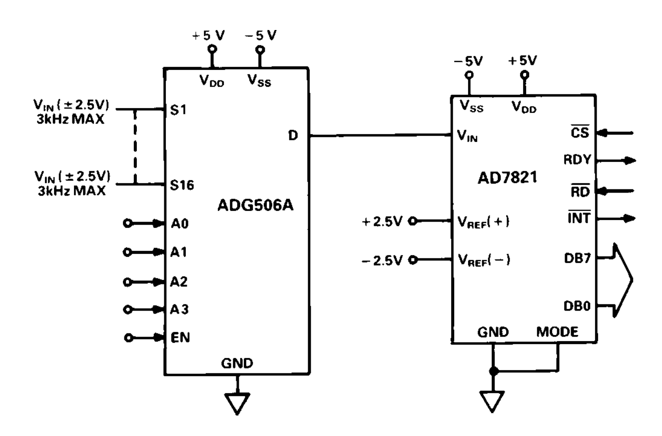


Figure 21. 16-Channel Telecom A/D Converter System

SIMULTANEOUS SAMPLING A/D CONVERTERS

The AD7821's inherent track-and-hold and well-defined sampling instant makes it useful, in such applications as sonar, where a number of input channels are required to be sampled simultaneously. Figure 22 shows a circuit for such an application.

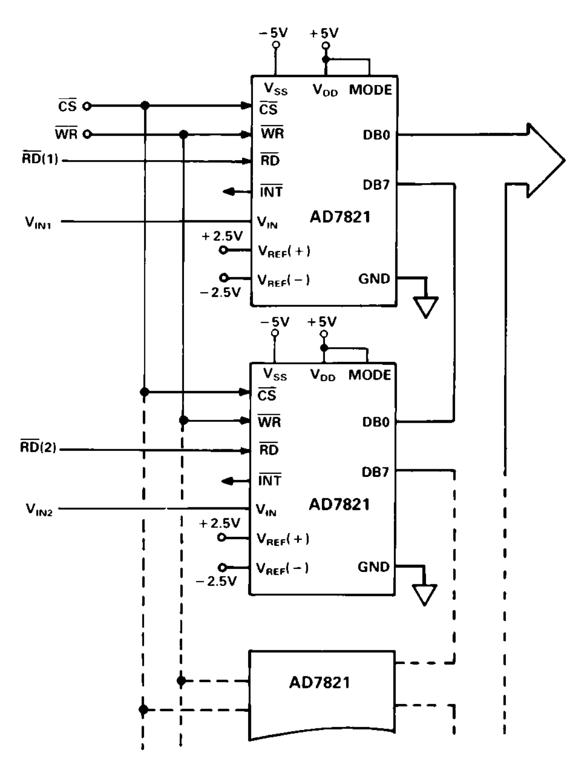


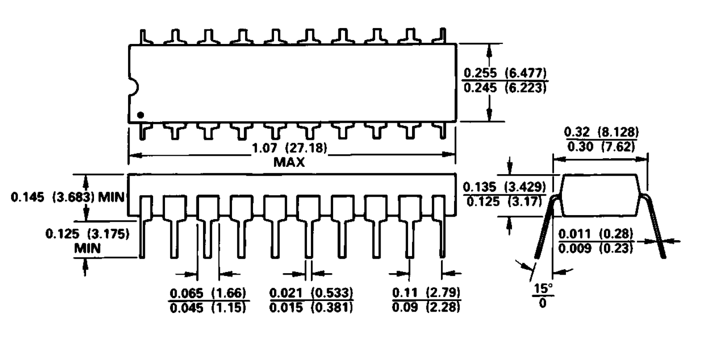
Figure 22. Simultaneous Sampling A/D Converters

The actual sampling instant, which is the instant at which V_{IN} is measured, occurs approximately 50 ns after the falling edge of WR or RD in the WR-RD or RD modes, respectively, due to internal logic delays. However, the internal logic delay and, therefore, the sampling instant can vary from device to device, but is typically within ±5 ns. This means that a maximum common input sine wave of ±2.5 V at 32 kHz, applied to any number of AD7821s in the circuit of Figure 22, will yield a maximum difference between the converter outputs of typically ±1/4 LSB.

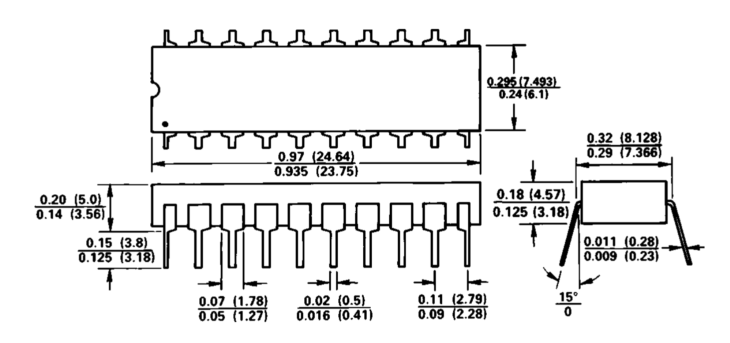
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

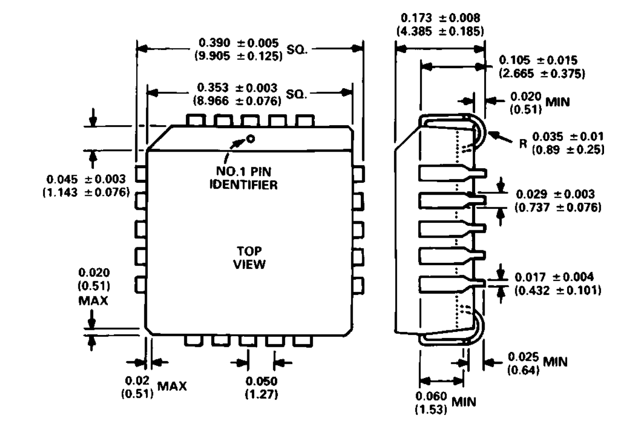
20-Pin Plastic DIP (N-20)



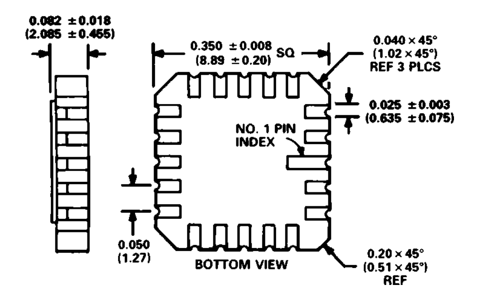
20-Pin Cerdip (Q-20)



20-Terminal Plastic Leaded Chip Carrier (P-20A)



20-Terminal Leadless Ceramic Chip Carrier (E-20A)



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